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An Efficient Reconfigurable Filter Design for Reducing Dynamic Power

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Abstract - This paper presents an architectural view of designing a digital filter. The main idea is to design a reconfigurable filter for reducing dynamic power consumption. By considering the input variation's we reduce the order of the filter considering the coefficient are fixed. The filter is implemented using mentor graphics using TSMC .18um technology. The power consumption is decreased in the rate of 16% from the conventional model with a slight increase in area overhead. If the filter coefficients are fixed then the power can be reduced up to 18% and the area overhead can also be reduced from the reconfigurable architecture.

***Key words*—** Low power digital filter, Reconfigurable filter**.**

1.INTRODUCTION

THE explosive growth in mobile computing and portable multimedia applications has increased the demand for low power digital signal processing (DSP) systems.

One of the most widely used operations performed in DSP is finite impulse response (FIR) filtering. The input-output relationship of the linear time invariant (LTI) FIR filter can be expressed as the following equation:

$$y(n) = \sum_{k=0}^{N-1} c_k \, x(n-k) \qquad (1)$$

Where N represents the length of FIR filter, the kth coefficient, and the x(n-k) input data at time instant. In many applications, in order to achieve high spectral containment and/or noise attenuation, FIR filters with fairly large number of taps are necessary.

Many previous efforts for reducing power consumption of FIR filter generally focus on the optimization of the filter coefficients while maintaining a fixed filter order. In those approaches, FIR filter structures are simplified to add and shift operations, and minimizing the number of additions/subtractions is one of the main goals of the research. However, one of the drawbacks in those approaches is that once the filter architecture is decided, the coefficients cannot be changed, those techniques are not applicable to the FIR filter with programmable coefficients.

Approximate signal processing techniques are also used for the design of low power digital filters. In [1], filter order dynamically varies according to the stop-band energy of the input signal. However, the approach suffers from slow filter-order adaptation time due to energy computations in the feedback mechanism. Previous studies in [2] show that sorting both the data samples and filter coefficients before the convolution operation has a desirable energy-quality characteristic of FIR filter. However, the overhead associated with the real-time sorting of incoming samples is too large.

In this paper, we propose a simple yet efficient low power reconfigurable FIR filter architecture, where the filter order can be dynamically changed depending on the amplitude of the filter inputs. In other words, when the data sample multiplied to the coefficient is so small as to mitigate the effect of partial sum in FIR filter, the multiplication operation can be simply cancelled. The filter performance degradation can be minimized by controlling the error bound as small as the quantization error or signal to noise power ratio (SNR) of given system. The primary goal of this work is to reduce the dynamic power of the FIR filter, and the main contributions are (1) A new reconfigurable FIR filter architecture with real-time input monitoring circuits is presented. Since the basic filter structure is not changed, it is applicable to the FIR filter with fixed coefficients or adaptive filters

The rest of the paper is organized as follows. In Section II, the basic idea of the proposed reconfigurable filter is described. Section III presents the reconfigurable fixed coefficient architecture and circuit techniques used to implement the filter.

2. RECONFIGURABLE FIR FILTERING TO TRADE OFF FILTER PERFORMANCE

In this section, we present direct form (DF) architecture of the reconfigurable FIR filter, which is shown in Fig. 1(a). In order to monitor the amplitudes of input samples and cancel the right multiplication operations, amplitude detector (AD) in Fig. 1(b) is used. When the absolute value of is smaller than the threshold *xth*, the output of AD is set to "1". The design of AD is dependent on the input threshold *xth*, where the fan in's of AND and OR gate are decided by *xth*. If *xth* and *cth* have to be changed adaptively due to designer's considerations, AD can be implemented using a simple comparator. Dynamic power consumption of CMOS logic gates is a strong function of the switching activities on the internal node capacitances.

In the proposed reconfigurable filter, if we turn off the multiplier by considering each of the input amplitude only, then, if the amplitude of input abruptly changes for every cycle, the multiplier will be turned on and off continuously, which incurs considerable switching activities. Multiplier control signal decision window (MCSD) in Fig. 1(a) is used to solve the switching problem. Using *ctrl* signal generator inside MCSD, the number of input samples consecutively smaller than are counted and the multipliers are turned off only when consecutive input samples are smaller than. Here, means the size of MCSD [in Fig. 1(a), is equal to 2].

Fig. 2(a) shows the *ctrl* signal generator design. As an input smaller than *xth* comes in and AD output is set to "1", the counter is counting up. When the counter reaches m, the *ctrl* signal in the figure changes to "1", which indicates that consecutive small inputs are monitored and the multipliers are ready to turn off. One additional m bit, in Fig. 2(a), is added and it is controlled by *ctrl*. The accompanies with input data all the way in the following flip-flops to indicate that the input sample is smaller than *xth* and the multiplication can be cancelled when the *cth* coefficient of the corresponding multiplier is also smaller than . Once the in_{cnt_in} signal is set inside MCSD, the signal does not change outside MCSD and holds the amplitude information of the input.

A delay component is added in front of the first tap for the synchronization between x*(n) and in Fig. 3(a) since one clock latency is needed due to the counter in MCSD. However, in the

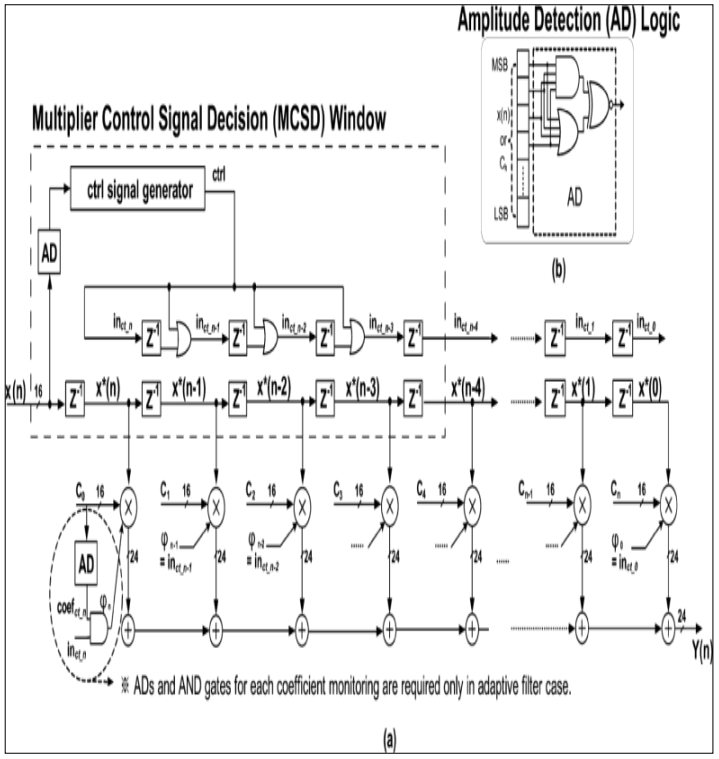

Figure. 1(a)MCSD window (b)Amplitude Detector

FIR filter with fixed or programmable coefficients, since we knowthe amplitude of coefficients ahead, extra AD modules for coefficient monitoring are not needed.

When the amplitudes of input and coefficient are smaller than *xth* and *cth* respectively, the multiplier is turned off by setting signal [Fig. 3(a)] to "1". Based on the simple circuit technique [11] in Fig. 4(b), the multiplier can be easily turned off and the output is forced to "0". As shown in the figure, when the control signal *ctrl* is "1", since PMOS turns off and NMOS turns on, the gate output is forced to "0" regardless of input.

When x_n is "0", the gate operates like standard gate. Only the first gate of the multiplier is modified and once this set to "1", there is no switching activity in the following nodes and multiplier output is set to "0". The area overheads of the proposed reconfigurable filter are flip-flops for signals, AD and *ctrl* signal generator inside MCSD and the modified gates in Fig. 2(b) for turning off multipliers.

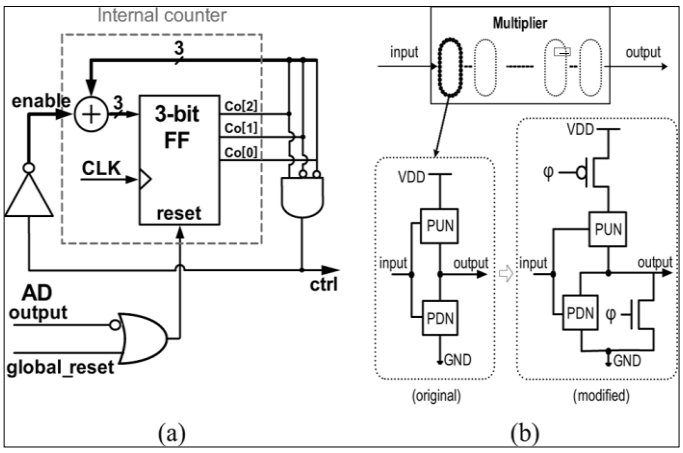

Figure. 2(a) Schematic of *ctrl* signal generator. Internal counter sets *ctrl* signal to "1" when all input samples inside MCSD are smaller than *xth* (m=4 case).(b) Modified gate schematic to turn off multiplier.

Those overheads can be implemented using simple logic gates, and a single AD is needed for input monitoring as specified in Fig. 1(a).

3. FIXED COEFFICIENT RECONFIGURABLE DIGITAL FILTER

The proposed reconfigurable digital filter uses the fixed coefficient. If we maintain a fixed coefficient then the power consumed by the multiplier for the various inputs are reduced by half literally. For example the C0=1100011 and the C11=1100011 then we can replace the coefficient of C11 with the C0. Thus the multiplication result of the C11 and C0 remains the same. This

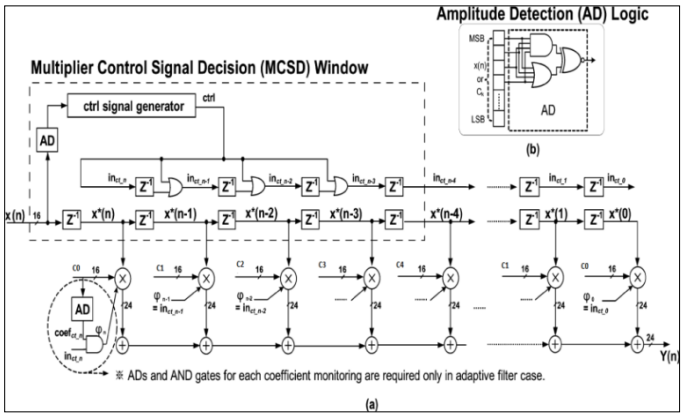

Figure. 3 Proposed FIR filter with fixed co-efficient

will reduce the multipliers switching activity.

This will enhance the power reduction. The power reduction achieved by the conventional, reconfigurable and fixed coefficient filter will reduce the power of the enormously. If the coefficients are fixed then significant reduction in area can be achieved. This can overcome one of the drawback of the filter as such area overhead. The results are shown in section IV.

4. RESULT

The reconfigurable digital filter is designed using the mentor graphics using TSMC .18um. The MCSD window which reduces the computation complexity by grouping the mitigate values. This in turn reduces the power by the 16% than that of conventional model.

TABLE 1 POWER AND AREA COMPARISON BETWEEN CONVENTIONAL, RECONFIGURABLE AND FIXED COEFFICIENT FIR FILTER

Parameter	Conventional	Reconfigurable	Fixed Coefficient Filter
Power (mW)	309	257	253
No. of Gate counts	2,702	2,017	1,993

There is a slight increase in area if the taps increases the area will be minimized. The simulation result of fixed coefficient filter is shown in fig.4 and the corresponding RTL schematic is shown in the fig.5. The result that we have obtained in the proposed method is shown in the table.1.

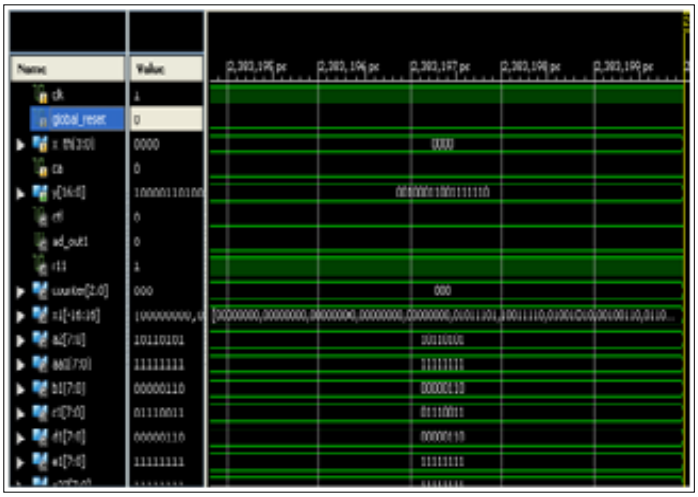

Figure. 4 Simulation result of fixed co-efficient filter

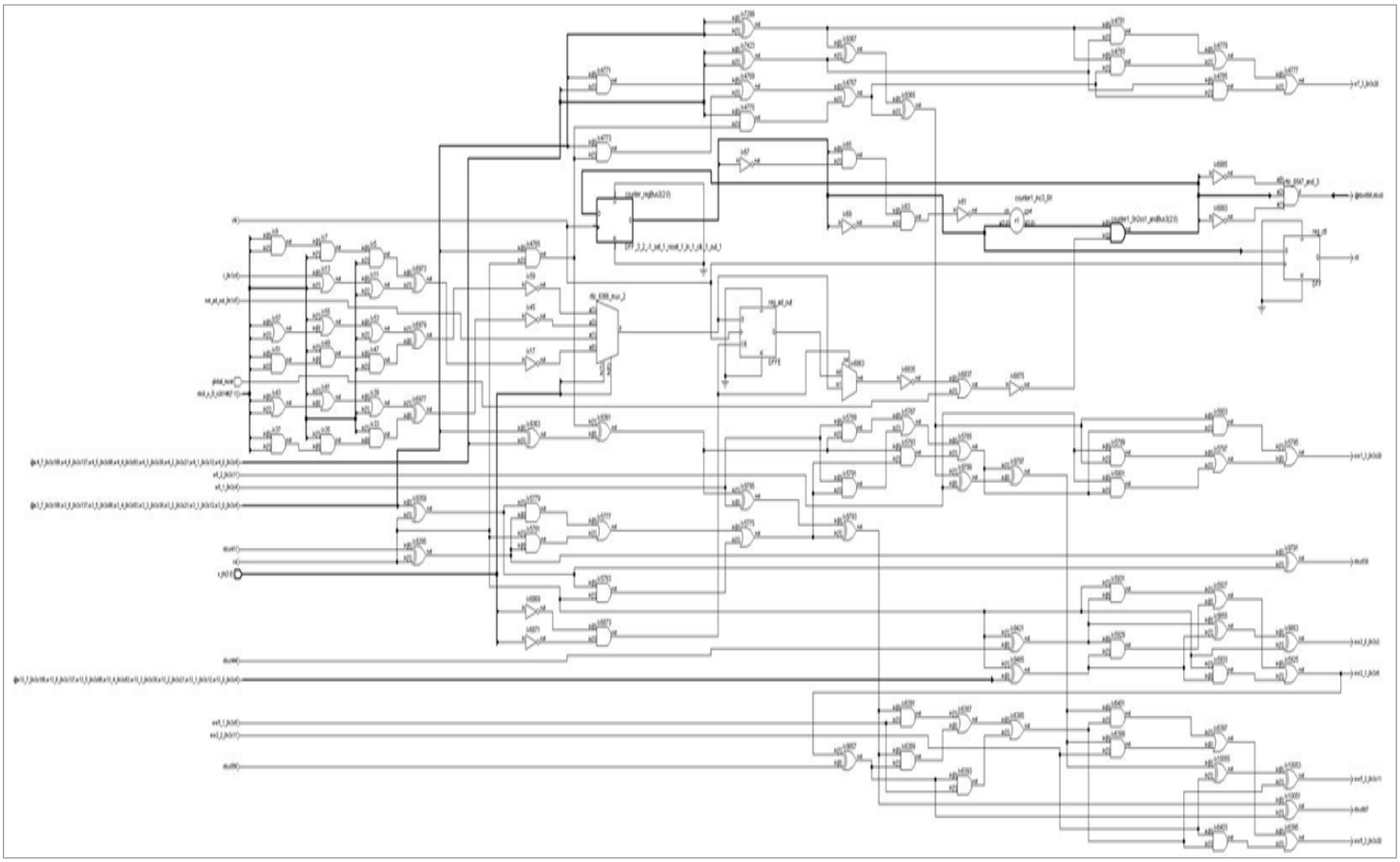

Figure. 5 RTL schematic of proposed fixed coefficient filter using TSMC .18 um technology

5. CONCLUSION

In this paper, we propose low power reconfigurable digital filter architecture. In the proposed reconfigurable filter, the input data are monitored and the multipliers in the filter are turned off when the coefficients inputs are small enough to mitigate the effect on the filter output. The power can be further reduced if the coefficients are fixed. The power reduced will be of 18%. The fixed coefficient can enhance the filters performance by reducing the power and the area.

The filter is designed using the using the VHDL code using the HDL designer from mentor graphics using TSMC .18um technology. We can implement the FIR filters in various fields such as general purpose computers, radars, wireless communication and audio processing applications. This This may enhance the systems performance by reducing the power.

6. ACKNOWLEDGEMENT

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